

A 10- μ W Digital Signal Processor with Adaptive-SNR Monitoring for a Sub-1V Digital Hearing Aid

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Abstract— An ultra low-power digital signal processor (DSP) is proposed for the digital hearing aid. The DSP has a SNR monitor to vary its internal clock frequency in accordance with the input signal level. Digital filters use hardwired barrel shifters in place of multipliers, and a parameter ROM provides filter parameters. The clock generator consumes only 1 μ W at sub-1V. The DSP consumes only 10 μ W at 0.9-V single supply, and occupies 0.3 mm² with gate count of 10k using 0.18- μ m CMOS process.

I. INTRODUCTION

Steadily increasing demands for digital hearing aids in the biomedical electronic system market needs low power operations, and many researches have been focused on reducing power consumption in hearing aid systems [1], [2]. This is because less power consumption translates into longer battery lifetime. General approaches to achieve low power consumption are to decrease the supply voltage level and/or the system clock frequency. However, lowering the voltage level and frequency is limited by signal-to-noise ratio (SNR) in hearing aid system, since it may result in degraded SNR, which is not suitable for hearing aid applications.

To solve this problem, we presented an analog front-end (AFE) using adaptive-SNR technique [3], [4] in which the clock frequency and the order of the sigma-delta modulator are varied according to the magnitude of the input sound signal. When the input signal level is sufficiently high we lowered the clock frequency to save the excessive power consumption. For the accurate monitoring of SNR values, only analog approach was used. However, the previous analog SNR detection logic had large load capacitance and was sensitive to thermal and flicker noise that lead to performance degradation.

In order to overcome these drawbacks of the analog approach, this paper proposes a noise-robust digital SNR monitor and integrates it into the digital signal processor (DSP) for the power reduction. Since the general purpose DSPs consume considerable power for SNR monitoring, a

new DSP is designed for flexibility as well as low power. Its low power architecture is based on energy-efficient algorithm and composed of low power ROM and a power efficient clock generator. In section II, the proposed system will be overviewed. Section III describes the design of the building blocks, and Section IV shows the simulation results. Finally, Section V concludes the paper.

II. SYSTEM OVERVIEW

Fig. 1 shows the overall architecture of the digital hearing aid system with the proposed DSP. As input signal passes through the SNR monitor, its amplitude is examined. Then, the monitor triggers the clock generator to vary its clock frequency. Initially the clock runs at high frequency (64 kHz). If the amplitude of the input signal is sufficiently large, the clock generator provides a low frequency (32 kHz) clock to the DSP. In addition, the AFE is triggered to adaptively choose the order of the internal sigma-delta modulator between 2 and 3. The high sound level of over 90-dB SPL is unlike in the case of normal sound level of 30 to 90-dB SPL and high performance processing is not required. By adaptively changing its processing performance in the each sound region, unnecessary power consumption can be removed [3], [4].

Fig. 2 shows the architecture of the proposed DSP. The input signal is divided into two separate frequency bands, high frequency (HI) and low frequency (LO) channels, separately processed, and then near the output terminal they

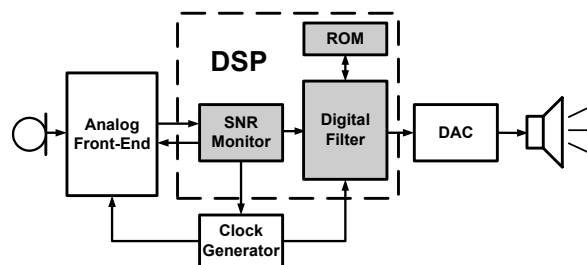


Figure 1. Hearing aid system with proposed DSP

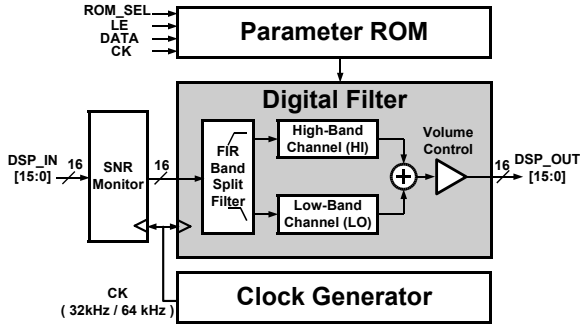


Figure 2. DSP Architecture

are merged to make a full band output signal. Unlike in the case of implantable cochlear system where the frequency bands are split into 16 or more channels, two channels are sufficient in this case [5]. This is because most of the patients, who have hearing problems, suffer from ski slope loss [5]. It is much worse in hearing high frequencies than in the lower frequencies. To compensate the ski slope loss, HI has a higher gain than LO does.

The DSP also has low-power ROM in which the parameters for the digital filter are stored. In addition, a low power clock generator is integrated for the overall DSP clocking.

III. BUILDING BLOCKS

A. Adaptive SNR Monitor

Fig. 3 shows the SNR monitor. In this case, SNR value is high when input sound signal is sufficiently large in magnitude. On the contrary, if the input signal has small amplitude, the quantization noise cannot be ignored and the SNR value is low. Therefore, SNR value of the input signal can be obtained by detecting the envelope of the input signal and comparing it with a threshold value.

Although the traditional envelope detection RC network can detect the envelope, it suffers from thermal and flicker noise, resulting in performance degradation. Moreover, capacitance in RC network plays as a heavy input load, making design of low power AFE difficult. Thus we used the digital envelope detector, reducing the input load and resolving the noise problem at the same time. Fig. 4 is the digital envelope detection algorithm [6], and Fig. 5 shows its results. The digital envelope detection works as follows:

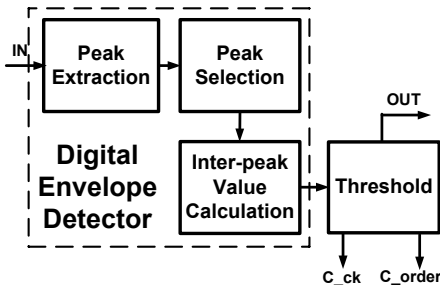


Figure 3. SNR monitor

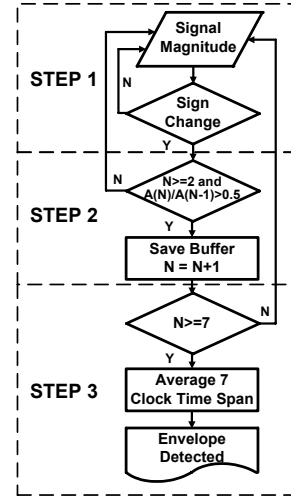


Figure 4. Digital envelope detection algorithm

TABLE I. SNR MONITOR OUTPUT SIGNALS

Input Amplitude (dB SPL)	0 – 90	90-100	100-105	> 105
C_ck	High	Low	High	Low
C_order	3 rd	2 nd	3 rd	2 nd

1) (STEP 1) Peak Extraction: The peaks of the input signal are extracted.

2) (STEP 2) Peak Selection: Among the positive peaks, only those with amplitude of at least half the size of the previous selected peak are selected and saved, as a and b of Fig. 5. Black dots are indicating selected peaks.

3) (STEP 3) Inter-peak Value Calculation: Inter-peak values are calculated by averaging the peak values inside of the 7-clock time span.

The threshold logic receives the detection results, and generates the clock control signal (C_ck) and the order control signal (C_order) according to the TABLE 1. The C_ck chooses the clock frequency between 32 kHz and 64 kHz while the C_order selects the order of the sigma-delta modulator in AFE between 2 and 3 [3], [4].

B. Adaptive Digital Filter with Gain Splitter

Fig. 6 presents the detail internal structure of the DSP. To

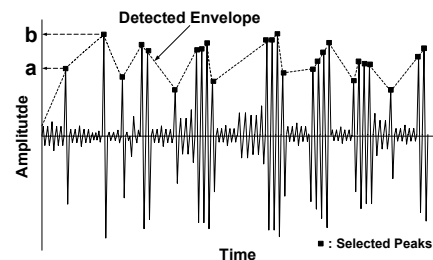


Figure 5. Digital envelope detection results

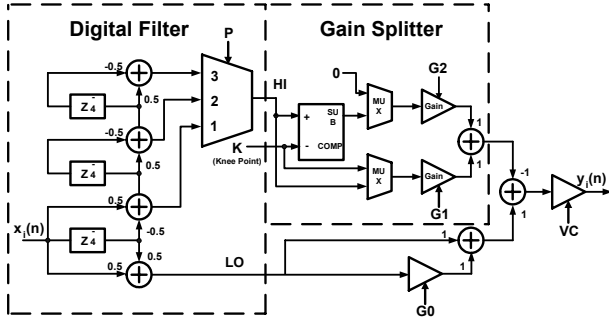


Figure 6. Digital Signal Processor

divide the input signal into 2 channels, we used a band-pass filter and a notch filter [7]. In contrast to the traditional band-splitting scheme with a low-pass and a high-pass IIR filters, this structure uses FIR filter and reduces power consumption and physical size for the similar results. This is because infinite impulse response (IIR) filter suffers from finite word-length problems and consumes more power than FIR [8]. Moreover, IIR has inevitable error accumulation and phase non-linearity problem which is not suitable for hearing aid applications.

For input signal $g(x)$, the filter function $F\{P, G_0, G_1, G_2, VC, K\}$ is determined so that output signal $o(x) = g(x) \cdot F$ shows flat characteristics throughout the frequency region. The parameter P determines the transition frequency from LO to HI channel. Parameter VC controls the volume. G_0 controls the gain in the region of LO, and the combination of G_1 and G_2 determines the gain of HI. In the graph of Fig. 7, the knee point K divides the linear region where G_1 controls the gain, and the compression region, where G_2 is in charge of the gain. That is to say, less gain is applied to the high magnitude signal than to the low magnitude signal. This is to prevent permanent hearing damage caused by loud and high frequency sound. The transfer function $H_T(z)$ of the DSP is given as

$$H_T(z) = VC [(1 + G_0) (0.5 + 0.5z^{-4}) - (KG_1 + G_2(IN - K)) (0.5 - 0.5z^{-4})^P] \quad (1)$$

In addition to channel division, elimination of the multipliers reduces the gate counts considerably and lowers power consumption further. This is because all of the coefficients in FIR filter are given as the powers of 2 making it possible to replace the multipliers with hardwired barrel shifters [7] for low power dissipation.

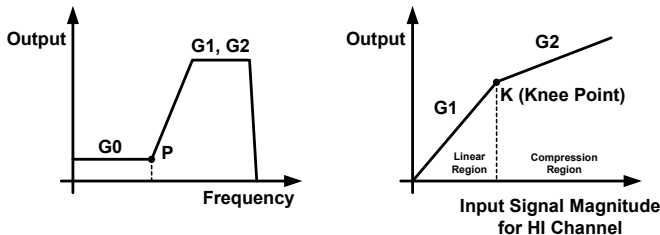


Figure 7. Programmable Parameters

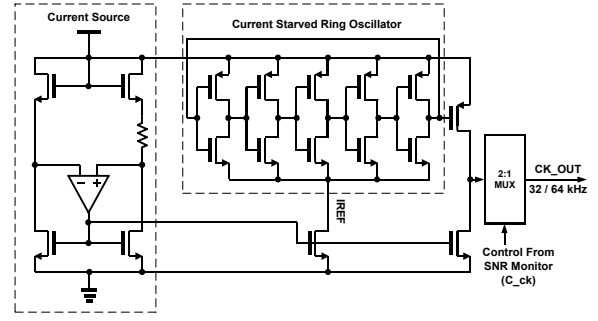


Figure 8. Clock Generator

C. Clock Generator

Current starved ring oscillator, often used in low-power oriented system, is used in the proposed low power clock generator. Typically, the supply voltage variation is suppressed by the cascode structure in the current source [9]. However, this structure limits the voltage headroom severely and is not applicable to this system which requires sub-1V operation. Hence the proposed clock generator, as shown in Fig. 8, uses the current source with an error amplifier in place of the cascode structure to relieve the voltage headroom limitation by reducing the number of stacked transistors. With this scheme, the MOSFET operates at sub-threshold region to make a linear feedback mechanism. The simulation results reveal that the clock generator can operate at supply voltage as low as 0.7 V, and dissipate only 1 μ W at 0.9-V. From the circuit, 64 kHz clock signal is generated, and the 2:1 clock divider with a 2:1 MUX is added at the output of the generator, supplying 32 kHz or 64 kHz to the system. The C_ck from the SNR monitor controls the 2:1 MUX.

D. Low Power Parameter ROM

The DSP gets the filter parameters from the low power ROM as shown in Fig. 9. Only NMOS transistors compose the ROM block, reducing the area compared with conventional type, where both PMOS and NMOS are used. Each bit line has a regenerating PMOS (M1 and M2) to fully charge the bit line up to the supply voltage level, preventing the unwanted threshold voltage drop caused by NMOS. Without any DC path, this scheme helps to minimize the static power consumption.

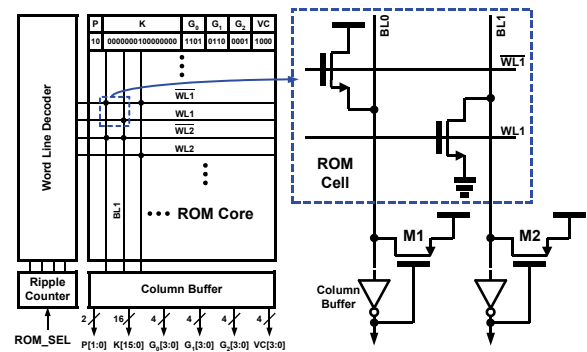


Figure 9. Parameter ROM

IV. IMPLEMENTATION RESULTS

The DSP is synthesized while the clock generator and the parameter ROM are layout by full-custom. Standard library cells of 1.8-V are used considering the estimated increase of gate delay at 0.9 V power supply. Simulation and verification are performed by using NanoSim-VCS. The chip layout is shown in Fig. 10. Excluding the pad, the chip area including the DSP, the parameter ROM and the clock generator is 0.3 mm² using 0.18- μ m CMOS technology. The gate count is 10k, and total power consumption of the DSP is 10- μ W at 0.9-V supply voltage. This system consumes 20% less power than the hearing aid system does without the proposed features, and the result shows a considerable power reduction compared with the previous work [1] for the similar performance.

Fig. 11 is the frequency compensated gain results of the proposed DSP. It is clear that the ski slope is compensated well by setting the optimized parameter values to control the signal gain. For the parameters of filter function F, we chose $F\{P, G0, G1, G2, VC, K\} = F\{3, 6, 2, 2, 8, 0\}$. SNR value versus the input signal of the DSP is plotted in Fig. 12. The input signal magnitude adaptively changes the clock frequency of the DSP and order of the AFE. Using the internal clock generator with low clock jitter provides 6-dB enhancement in measured SNR value compared with our previous works [3], [4]. Simulation results of the hearing aid system with the proposed DSP is shown in Fig. 13. The input signal is 4.2 kHz with magnitude of 70 mV_{p-p}. Total processing time of the hearing aid system with the proposed DSP is less than 1msec. This is short enough to prevent a patient to be confused with the time-lag between lip-reading and listening induced by the delay.

V. CONCLUSION

A low power DSP with adaptive-SNR monitoring is

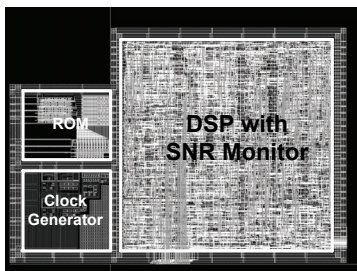


Figure 10. Chip Layout (0.3mm² without pads)

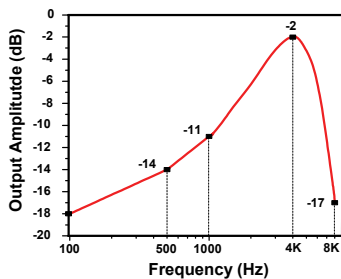


Figure 11. Frequency gain compensation of the DSP

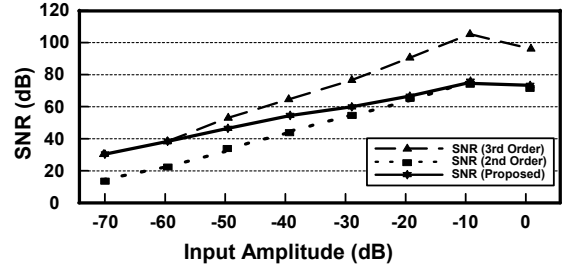


Figure 12. SNR vs. Input

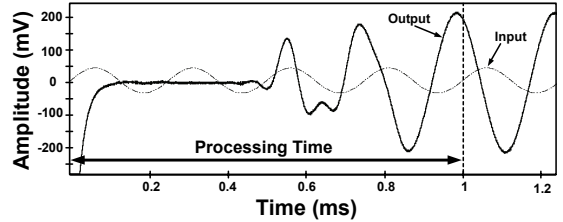


Figure 13. Processing time of the hearing aid system

proposed, designed, implemented and measured for a sub-1V digital hearing aid. It integrates the SNR monitoring and energy-efficient algorithm, combined with the low power clock generator and a low power parameter ROM, consumes only 80% of the overall power of the digital hearing aid system without them. The DSP block and the clock generator all operate at 0.9-V supply voltage and consume only 10 μ W and 1 μ W, respectively. At 0.18- μ m process, the chip area is 0.3 mm² while the gate count is 10k.

REFERENCES

- [1] H. Neuteboom, Ben M. J. Kup, and M. Janssens, "A DSP-Based Hearing Instrument IC", *IEEE J. Solid-State Circuits*, Vol. 32, No. 11, Dec. 1997.
- [2] Francisco Serra-Graells, Lluís Gomez, and José L. Huertas, "A Ture-1-V 300- μ W CMOS-Subthreshold Log-Domain Hearing-Aid-On-Chip", *IEEE J. Solid-State Circuits*, Vol. 33, No. 8, Aug. 2004.
- [3] S. Kim, J.-Y. Lee, S.-J. Song, N. Cho, and H.-J. Yoo, "An Energy-Efficient Analog Front-End Circuit for a Sub-1V Digital Hearing Aid Chip", *IEEE Symposium on VLSI Circuits, Dig. Tech. Papers*, pp.176-178, Jun. 2005.
- [4] S. Kim, J.-Y. Lee, S.-J. Song, N. Cho, and H.-J. Yoo, "A 0.9-V 67 μ W Analog Front-End using Adaptive-SNR Technique for Digital Hearing Aid", *IEEE Symposium on Circuits and Systems*, May 2005.
- [5] P. Yanick and Harris Drucker, "Signal Processing to Improve Intelligibility in the Presence of Noise for Persons with a Ski-Slope Hearing Impairment", *IEEE Trans. on Acoustics, Speech, and Signal Processing*, Dec. 1976.
- [6] J. Y. Lee, J. K. Kim and G. Yoon, "Digital envelope detector for blood pressure measurement using an oscillometric method", *J. Medical Engineering & Technology*, Vol. 26, No.3, pp. 117-122, May/June 2002.
- [7] Walter P. Sjrursen, "Hearing aid digital filter", *U.S. Patent 6 292 571 B1*, Sep. 2001
- [8] Emmanuel C. Ifeakor and Barrie W. Jervis, "Digital Signal Processing 2nd Edition", *Pretence Hall*, p. 321
- [9] N. Cho, S.-J. Song, J. Lee, S. Kim, S. Kim, and H.-J. Yoo, "A 5.1- μ W UHF RFID Tag Chip integrated with Sensors for Wireless Environmental Monitoring", *IEEE European Solid-State Circuits Conference*, pp. 279-282, Sep. 2005.